REMARKS

Supplemental Information Disclosure Statement

Applicant respectfully brings to the Examiner's attention the Supplemental Information Disclosure Statement filed herewith.

Claims 1-4

New claims 3 and 4 are added to claim further aspects of the invention, and claims 1-4 are pending in this application.

The Office Action does not establish that claims 1-2 are unpatentable under 35 USC §103(a) over "Gardner" (US patent no. 5,885,874 to Gardner) in view of "Mizutani" (US patent no. 4,661,833 to Mizutani). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for combining the teachings of Gardner with teachings of Mizutani, and fails to show that the combination could be made with a reasonable likelihood of success.

As to claim 1, the Office Action alleges that "Gardner does not specifically describe the process as programming a memory cell and applying the programming voltage as claimed ... [but does teach] that the process can be applied to a memory." This reading of Gardner is thought to state more than Gardner actually teaches. The cited paragraph at col. 10, ll. 30-40 of Gardner reads:

> The invention is particularly well-suited for fabricating N-channel MOSFETs, P-channel MOSFETs and other types of IGFETs, particularly for high-performance microprocessors where high circuit density is essential. Although a single pair of enhancement-mode and depletion-mode devices has been shown for purposes of illustration, it is understood that in actual practice, many devices are fabricated on a single semiconductor wafer as widely practiced in the art. Accordingly, the invention is well-suited for use in an integrated circuit chip, as well as an electronic system including a microprocessor, a memory and a system bus.

It is respectfully submitted that the paragraph clearly states that Gardner's invention is well-suited for fabricating N-channel MOSFETs, P-channel MOSFETs and other types of IGFETs, particularly for high-performance microprocessors. The paragraph goes on in a general statement that Gardner's invention is suited for an "electronic system

including a microprocessor, a memory and a system bus." Thus, there is no apparent specific indication that Gardner's invention can be applied to programming a memory. Even if Gardner was to be construed as suggesting that a memory cell can be made by his process (which Applicant does not concede), that is not a suggestion that Gardner's process could be used to program a memory cell. Gardner appears to teach that his invention is well-suited for fabricating N-channel MOSFETs, P-channel MOSFETs and other types of IGFETs, particularly for high-performance microprocessors, and a system that may include a memory. There is no suggestion that Gardner's invention would or could be used to program a memory.

As to claim 2, the Office Action alleges that "Gardner can be configured to have silicide agglomerated over the channel region." However, the Office Action fails to present any evidence presented to support this allegation. Simply alleging that Gardner's structure "can" be modified does not suggest that one would actually do so. Therefore, the Office Action fails to show that the prior art suggests applying a programming voltage across the metal silicide layer, the metal silicide layer being configured to agglomerate over the channel region when subjected to the programming voltage.

The alleged motivation for combining Gardner with Mizutani is improper. In support of combining the references, the Office Action indicates that "it would have been obvious ... to incorporate the process disclosed by Gardner as part of the programming process on the memory cell as taught by Mizutani because Gardner suggested that numerous variations can be provided and both references show different threshold voltages." Not only is the alleged motivation conclusory, but the asserted combination would change the principle of operation of Mizutani.

Gardner teaches annealing to drive-in and activate implanted dopants, and makes no apparent suggestion of doing so for programming a memory cell. Mizutani teaches an EEPROM having a floating gate structure. It is respectfully submitted that those skilled in the art would recognize that even if Gardner could be construed as teaching the programming of a memory cell with his fabrication process, such programming would appear to obviate the need for Mizutani's floating gate structure in an EEPROM. Thus, combining Gardner's teachings with those of Mizutani would

change a principle of operation of Mizutani. Therefore, the alleged motivation is improper because the proposed modification cannot change the principle of operation of a reference (MPEP §2143.01).

The rejection of claims 1 and 2 over the Gardner-Mizutani combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

New claims 3 and 4 distinguish over the cited prior art for at least the reasons of claims 1 and 2, from which they depend.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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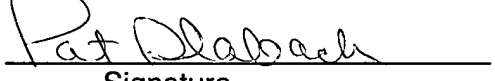
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